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EXAMINER	
CHERY, MARDOCHEE	

ART UNIT	PAPER NUMBER
2186	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/662,225	PLESSIER ET AL.	
	Examiner	Art Unit	
	MARDOCHEE CHERY	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-9 and 12-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-9 and 12-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office action is a reply to Applicant's communication filed July 10, 2009 in response to the Office action mailed April 2, 2009. In response to the last Office action, claims 3, 8-9, 12 and 14 have been amended. Claim 10 is now canceled. As a result, claims 2, 3-9, and 12-20 are now pending.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on November 12, 2003, with reference EP 0 295 751, is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

3. The objection to the specification is withdrawn in view of the amendment filed July 10, 2009.

Claim Objections

4. The objection to claim 8 is withdrawn in view of the amendment filed July 10, 2009.

Claim Rejections - 35 USC § 112

5. The rejection of claim 10 under 35 U.S.C. 112, first paragraph is withdrawn by virtue of its cancellation.

Response to Arguments

6. Applicant's arguments filed July 10, 2009 have been fully considered but they are not persuasive.

a. In regards to claim 8, Applicant's representative argues on page 10, paragraph 3 of the remarks that Stone does not disclose "a control circuit operable to provide random access to memory locations responsive to a read operation and to provide sequential access to the memory locations responsive to a write operation".

Examiner respectfully disagrees. Stone discloses "a controller determining whether either a read request or a write request has been received and retrieving the requested information sequentially or randomly based on whether the request is a read request or a write request [col. 9, lines 36-38; 44-46; 53-54; 58-62]. Fig. 10 further illustrates the aspect of "providing random access responsive to a read operation and sequential access responsive to a write operation" for example in step 1010 where the controller determines whether the request is a "Read Request", if Yes/Read, in step 1026, then randomly retrieve data in step 1034. On the other hand, in step 1014, if the request is a write request (i.e., Yes/Write), Write Data Sequentially in step 1022.

Nojiri also discloses "a memory which provides a random read and sequential write mode for read and write operations; col. 12, lines 39-41.

b. With respect to claim 8, Applicant's representative further argues on page 10, paragraph 3, that Stone "allows both read operations and write operations to occur using either random access or sequential access".

However, it is worth mentioning that the recitation of "provide random access responsive to a read operation and provide sequential access responsive to a write operation", in claim 8, does not prevent having sequential access in response to a read operation or random access responsive to a write operation, or vice versa.

c. With respect to claim 14, Applicant's representative further argues on page 10, paragraph 4 of the remarks, that "claim 14 as amended is patentable at least for the reasons described above with respect to claim 8".

Claim 14 recites, in relevant part, "force random access to the memory locations responsive to a read operation and force sequential access to the contents of the memory locations via one of the memory locations responsive to a write operation". Fig. 10 of Stone illustrates the aspect of "force random access responsive to a read operation and force sequential access responsive to a write operation" for example in step 1010 where the controller determines whether the request is a "Read Request", if Yes/Read, in step 1026, then randomly retrieve data in step 1034. On the other hand, in step 1014, if the request is a write request (i.e., Yes/Write), Write Data Sequentially in step 1022.

Nojiri also discloses "a memory which provides a random read and sequential write mode for read and write operations; col. 12, lines 39-41.

d. With respect to claim 8, Applicant's representative further argues on page 11, paragraph 5 of the remarks that Nojiri discloses that the "read and write operations…are achieved under a random read and sequential write mode" but does not describe how these operations are achieved.

Examiner would like to point out that Applicant is not claiming how "a random read operation" and "a sequential write operation" are performed, rather simply "provide/force random access responsive to a read operation and provide/force sequential access responsive to a write operation" as shown in claims 8 and 14. Thus Nojiri discloses the limitations of claims 8 and 14, at least in col. 12, lines 39-41, wherein "a random read mode is achieved in response to read operations and a sequential write mode is achieved is achieved in response to write operations". Applicant's representative arguments regarding "Nojiri does not describe how these operations are achieved" have no bearing on whether "random access is provided in response to a read operation" or "sequential access is provided in response to a write operation".

e. Applicant's representative argues on page 12, paragraph 1, with respect to claim 8, that Nojiri and Tomaiuolo are completely non-analogous art.

In response to applicant's argument that "Nojiri and Tomaiuolo are completely non-analogous art", it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably

pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, both Nojiri and Tomaiuolo deals with operation modes of a memory device, that is how data is read from the memory in a read mode and how data is written to that memory in a write mode (See Nojiri @ col. 5, lines 34-36; Tomaiuolo @ Abstract, paragraph [0001]).

In view of the Supreme Court decision in KSR International Co. v. Teleflex Inc., Examiner would like to point out that, in determining obviousness under 35 U.S.C 103, the Supreme Court stated that: "When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill".

Still further, the court states that "the focus when making a determination of obviousness should be on what a person of ordinary skill in the pertinent art would have known at the time of the invention…and this is regardless of whether the source of that knowledge and ability was documentary prior art, general knowledge in the art, or common sense".

Finally, for purposes of 35 U.S.C 103, prior art can be either in the field of applicant's endeavor or be reasonably pertinent to the particular problem with

which the applicant was concerned. Furthermore, prior art that is in a field of endeavor other than that of the applicant, or solves a problem which is different from that which the applicant was trying to solve, may also be considered for the purposes of 35 U.S.C 103. See, e.g., In re *KSR International Co. v. Teleflex Inc.,* 550 U.S. at_,82 USPQ2d at 1396 (2007).

f. Applicant's representative argues on page 13 of the remarks with respect to claim 3 that APA discusses FIFO memories and randomly-accessible memories, but does not disclose a memory that is configurable between those two options as separate modes of operation.

Examiner would like to point out that, in the Office action mailed April 2, 2009, APA was relied upon for teaching " a first operating configuration, in which the memory elements of the at least one array are coupled one to another to form a monodimensional sequentially-accessible memory, and a second operating configuration, in which the memory elements in each sub-array are coupled to one another so as to form an independent monodimensional sequentially-accessible memory block". What defines "a first operating configuration" in claim 3 is that, in that first configuration, "the memory elements of the at least one array are coupled one to another to form a monodimensional sequentially-accessible memory" and what defines "a second operating configuration" is in that second configuration "the memory elements in each sub-array are coupled to one another so as

to form an independent monodimensional sequentially accessible memory block". Thus, APA meets both of these limitations by virtue of disclosing "a FIFO memory including a monodimensional array of memory elements, and can only be accessed sequentially" [par. 6].

g. Applicant's representative further argues on page 14, with respect to claim 3, that Stone neither discloses nor suggests "placing a memory into one of two operating configurations depending on whether data is being stored therein or retrieved therefrom".

Examiner respectfully disagrees. Claim 3 does not positively recite "placing the memory into one of two configurations…" Rather, claim 3 describes "the first configuration as a configuration in which the memory is placed when (i.e., if) data are to be stored therein" and "the second configuration as a configuration in the memory is placed when (i.e., if) data are to be retrieved therefrom". Thus, the act of placing the memory into one of two configurations may not occur if no data are to be stored or retrieved.

Additionally, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "placing a memory into one of two operating configurations depending on whether data is being stored therein or retrieved therefrom") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not

read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Furthermore, Stone discloses [Fig. 10, *step 1010 read request?, yes/read, step 1026 random?, random: step 1034 read/retrieve data*; col. 9, lines 43-46, 58-64; Fig. 10, *step 1010 Read/Write Request?: if Yes/Read then step 1030: Retrieve Data Sequentially or step 1034: random retrieve data using address; or if Yes/write, then step 1018: random write data to address or step 1022: Write Data Sequentially*; col. 9, lines 36-64], [Fig. 10, *step 1010 write request, Yes/write, step 1022 write data sequentially*; col. 10, lines 8-12].

h. Applicant's representative argues on page 15 of the remarks, with respect to claim 12, that Stone neither discloses nor reasonably suggests "a control circuit operable to cause a memory array to operate as a random-access memory during all read operations, and as a first-in-first-out memory during all write operations".

Examiner respectfully disagrees. Claim 12 recites, in pertinent part, "a control circuit operable to cause a memory array to operate as a random-access memory during all read operations, and as a first-in-first-out memory during all write operations". Examiner would like to point out that the claim language (a control circuit operable to cause a memory array to operate ...) allows Stone to read meet the claimed limitation for the controller in Stone is operable to cause the memory to operate as random-access memory during all read operations. For instance, if request is "Yes/Read" in step 1010 of Fig. 10, the controller 516 of Fig. 5 is operable

to cause step 1026 to be "Random" for every read request to retrieve data. Likewise, if the Request is "Yes/Write" in step 1010 of Fig. 10, the controller 516 of Fig. 5 is operable to cause step 1014 to be "FIFO" for every write requests. Thus, the controller 516 of Fig. 5 is operable to cause the memory to operate as a random-access memory during all read operations, and as a first-in-first-out memory during all write operations.

i. The rejections have been modified to address the latest claim amendments including additional claim rejections or objections introduced by the last amendments. The latest amendment, however, does not remove the references from reading upon the claims.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claims 8-9, 12-14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. See Waldemar Link, GmbH & Co. v. Osteonics Corp. 32 F.3d 556, 559, 31 USPQ2d 1855, 1857 (Fed. Cir. 1994); In re

Rasmussen, 650 F.2d 1212, 211 USPQ 323 (CCPA 1981). See MPEP § 2163.06 - § 2163.07(b) for a discussion of the relationship of new matter to 35 U.S.C. 112, first paragraph.

j. In particular claims 8-9 recite "provide random access to the memory locations responsive to a read operation and provide sequential access to the memory locations responsive to a write operation". These limitations find no support in the original disclosure as required by 35 USC 112 first paragraph and consist new matter. Though the original disclosure provides for "allowing random access to the memory locations during a read mode of operation, and allowing sequential access to the memory locations during a write mode of operation" in original claim 8, and paragraph [57], it does not provide support for "providing random access to the memory locations responsive to a read operation and providing sequential access to the memory locations responsive to a write operation". The word "allow", when interpreted in light of the specification, appears to be of different scope than "provide".

k. In particular, claims 12-13 recite "a control circuit operable to cause the array to operate as a random-access memory during all read operations, and a first-in-first-out memory during all write operations". These limitations are not supported by the original disclosure. The disclosure in original claims 8 and simply provides for "a control circuit operable to, allow random access to the memory locations during a first mode of operation, and allow sequential access to the contents of the memory locations via a predetermined one of the memory

locations during a second mode of operation, wherein the first mode of operation comprises a read mode and the second mode of operation comprises a write mode".

l. In particular claim 14 recites "force random access to the memory locations responsive to a read operation, and force sequential access to the contents of the memory locations responsive to a write operation". Though the original disclosure provides for "allowing random access to the memory locations during a first mode of operation, and allowing sequential access to the memory locations during a write mode of operation" in original claim 8, and paragraph [57], it does not provide support for "forcing random access to the memory locations responsive to a read operation and forcing sequential access to the memory locations responsive to a write operation". The word "allow", when interpreted in light of the specification, appears to be of different scope than the word "force". In this case, the word "allow" permits more than one possibility while "force" is constricted to just one choice.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claims 8-9 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

m. In particular, claims 8-9 recite in pertinent part, "provide random access to the memory locations responsive to a read operation and provide sequential access to the memory locations responsive to a write operation". It is unclear what is meant intended by those limitations. The invention pertains to randomly reading from a memory and sequentially writing to the memory. However, as used in the claims, the term "provide" connotes that access has been blocked to the memory locations and that it is "responsive to a read operation or a write operation" is what provides access to the memory locations. As such, these limitations render the claims indefinite and ambiguous. However, for examination purposes, the broadest reasonable interpretation is in view where "providing random access or sequential access will be construed as "randomly reading from a memory and sequentially writing to the memory".

n. Claim 14 recites in pertinent part "force random access to the memory locations responsive to a read operation, and force sequential access to the contents of the memory locations via one of the memory locations responsive to a write operation". The use of the term "force" in this context renders the claims ambiguous and indefinite for it is unclear what is meant by "forcing random access and forcing sequential access". The term force implies that access has been prohibited to the contents of the memory locations. However, as shown in the specification the invention does not deal with blocking access, providing access, or forcing access to memory locations, rather "randomly reading from a

memory and sequentially writing to the memory". Thus, claim 14 will be construed to that regard.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

12. Claims 8-9 and 15-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Stone et al. (6,578,109).

As per claim 8, Stone et al. discloses a memory [Fig. 5, *cache 368*], comprising: a plurality of memory locations [Fig. 5, *cache registers 524*; col. 6, lines 47-49]; and a control circuit coupled to the memory [Fig. 5, *cache controller 516*; col. 6, lines 29-34] and operable to, provide random access to the memory locations responsive to a read operation [Fig. 10, *step 1010 read request?, yes/read, step 1026 random?, random: step 1034 read/retrieve data*; col. 9, lines 43-46, 58-64], and provide sequential access to the memory locations responsive to a write operation [Fig. 10, *step 1010 write request, Yes/write, step 1022 write data sequentially*; col. 10, lines 8-12].

As per claim 9 Stone discloses the control circuit provides sequential access to the memory locations during the write operation so that the memory functions as a first-in-first-out memory [col. 10, lines 8-12].

As per claim 15, Stone et al. discloses a method, comprising: randomly accessing memory locations of a memory during either a read mode or a write mode of operation [Fig. 10, *step 1010 read/write request?, yes/read, step 1026 random?, random: step 1034 read/retrieve data; Yes/write, step 1014 random write data to address*; col. 9, lines 43-46, 58-64], and sequentially accessing the memory locations via one of the memory locations during the read or write mode of operation [Fig. 10, *step 1030, retrieve data sequentially; step 1022, write data sequentially*; col. 10, lines 8-18], wherein the sequentially accessing occurs during the alternate mode of operation as does the randomly accessing [Fig. 10, *step 1010 Read/Write Request?: if Yes/Read then step 1030: Retrieve Data Sequentially or step 1034: random retrieve data using address; or if Yes/write, then step 1018: random write data to address or step 1022: Write Data Sequentially*; col. 9, lines 36-64].

As per claim 16, Stone et al. discloses wherein randomly accessing the memory locations comprises: accessing a first memory location having a first address [col. 11, lines 57-58]; and accessing a second memory location having a second address [col. 11, lines 61-62].

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stone (6,578,109) and Iadanza (6,091,645).

As per claim 17, Stone discloses the invention as claimed with respect to claim 15. Stone further discloses reading first data from a first memory location [Fig. 10, col. 9, lines 43-46]; and reading the second data from the first memory location [col. 9, lines 45-51], but does not explicitly disclose shifting second data from a second memory location into the first memory location.

Iadanza, however, discloses shifting second data from a second memory location into the first memory location [col. 8, ll 36-50; col. 10, ll 29-42; col.11, ll 28-35; col. 35, ll 52-59].

Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Stone et al., to include shifting second data from a second memory location into the first memory location because doing so would have provided serial scan shifting of data for driving each of the memory cells (col. 11, ll 30-35) as taught by Iadanza.

As per claim 18, Stone discloses the invention as claimed with respect to claim 15. Stone further discloses writing first data to a first memory location [col. 10, lines 8-11]; writing second data to the first memory location [col. 10, lines 10-18], but does not explicitly disclose shifting the first data from the first memory location to a second memory location.

Iadanza discloses shifting the first data from the first memory location to a second memory location [col. 8, ll 36-50; col. 10, ll 29-42; col.11, ll 28-35; col. 35, ll 52-59].

Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Stone et al., to include shifting the first data from the first memory location to a second memory location because doing so would have provided serial scan shifting of data for driving each of the memory cells (col. 11, ll 30-35) as taught by Iadanza.

As per claim 19, Stone discloses the invention as claimed with respect to claim 15. Stone, however, does not explicitly disclose shifting the contents of each respective memory location to a respective next memory location a number of times; and accessing a predetermined one of the memory locations after a predetermined one of the shifts.

Iadanza discloses shifting the contents of each respective memory location to a respective next memory location a number of times [col. 8, ll 36-50; col. 10, ll 29-42; col.11, ll 28-35; col. 35, ll 52-59]; and accessing a predetermined one of the memory

locations after a predetermined one of the shifts [col. 8, ll 36-50; col. 10, ll 29-42; col.11, ll 28-35; col. 35, ll 52-59].

Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Stone et al., to include shifting the contents of each respective memory location to a respective next memory location a number of times; and accessing a predetermined one of the memory locations after a predetermined one of the shifts because doing so would have provided serial scan shifting of data for driving each of the memory cells (col. 11, ll 30-35) as taught by Iadanza.

As per claim 20, Stone discloses the invention as claimed with respect to claim 15, Stone, however, does not explicitly disclose shifting the contents of each of n respective memory locations to a respective next one of the n memory locations n times; and accessing a predetermined one of the n memory locations after a predetermined one of the n shifts.

Iadanza discloses shifting the contents of each of n respective memory locations to a respective next one of the n memory locations n times [col. 8, ll 36-50; col. 10, ll 29-42; col.11, ll 28-35; col. 35, ll 52-59]; and accessing a predetermined one of the n memory locations after a predetermined one of the n shifts [col. 8, ll 36-50; col. 10, ll 29-42; col.11, ll 28-35; col. 35, ll 52-59].

Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Stone et al., to include shifting the

contents of each of n respective memory locations to a respective next one of the n memory locations n times; and accessing a predetermined one of the n memory locations after a predetermined one of the n shifts because doing so would have provided serial scan shifting of data for driving each of the memory cells (col. 11, ll 30-35) as taught by Iadanza.

15. Claim 8 and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomaiuolo (2002/0087817) and Nojiri (4,656,625).

As per claim 8, Tomaiuolo discloses a memory, comprising: a plurality of memory locations [par. 006]; and a control circuit coupled to the memory [page 6, left column, par. 8].

Tomaiuolo does not explicitly disclose a control circuit operable to, provide random access to the memory locations responsive to a read operation, and provide sequential access to the memory locations responsive to a write operation.

Nojiri, however, discloses a control circuit operable to, provide random access to the memory locations responsive to a read operation, and provide sequential access to the memory locations responsive to a write operation [col. 12, lines 39-42; col. 13, lines 54-56].

Thus, it would have been obvious to one of ordinary skill in the art, at the time of invention by applicant, to modify the system of Tomaiolo to include a control circuit operable to, provide random access to the memory locations responsive to a read

operation, and provide sequential access to the memory locations responsive to a write operation because doing so would have indicated how data should be read from the memory in a read mode and how data should be written to that memory in a write mode (col. 5, lines 34-36) as taught by Nojiri.

As per claim 14, Tomaiuolo discloses an electronic system, comprising: a plurality of memory locations [par. 006]; and a control circuit coupled to the memory locations [page 6, left column, par. 8].

Tomaiuolo does not explicitly disclose a control circuit operable to, force random access to the memory locations responsive to a read operation, and force sequential access to the contents of the memory locations via one of the memory locations responsive to a write operation.

Nojiri, however, discloses a control circuit operable to, force random access to the memory locations responsive to a read operation, and force sequential access to the contents of the memory locations via one of the memory locations responsive to a write operation [col. 12, lines 39-42; col. 13, lines 54-56].

Thus, it would have been obvious to one of ordinary skill in the art, at the time of invention by applicant, to modify the system of Tomaiolo to include a control circuit operable to, force random access to the memory locations responsive to a read operation, and force sequential access to the contents of the memory locations via one of the memory locations responsive to a write operation because doing so would have

indicated how data should be read from the memory in a read mode and how data should be written to that memory in a write mode (col. 5, lines 34-36) as taught by Nojiri.

As per claim 15, Tomaiuolo discloses a method comprising randomly accessing memory locations of a memory during either a read mode or a write mode of operation, and sequentially accessing the memory locations via one of the memory locations during the read or write mode of operation [par. 0004, page 6, claim text 1]. However, Tomaiuolo does not explicitly disclose wherein the sequential accessing occurs during the alternate mode of operation as does the randomly accessing.

Nojiri discloses the sequential accessing occurs during the alternate mode of operation as does the randomly accessing [col. 12, lines 39-42; col. 13, lines 54-56].

Thus, it would have been obvious to one of ordinary skill in the art, at the time of invention by applicant, to modify the system of Tomaiolo to include the sequential accessing occurs during the alternate mode of operation as does the randomly accessing because doing so would have indicated how data should be read from the memory in a read mode and how data should be written to that memory in a write mode (col. 5, lines 34-36) as taught by Nojiri.

As per claim 16, Tomaiuolo discloses randomly accessing the memory locations comprises accessing a first memory location having a first address [par. 0011]; and accessing a second memory location having a second address [par. 0011].

16. Claims 2-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iadanza (6,091,645), Applicant Admitted Prior Art (hereinafter APA), and Stone (6,578,109).

As per claim 3, Iadanza discloses a memory comprising: at least one array of memory elements [col. 2, ll 28-35]; a partition of the at least one array into a plurality of sub-arrays of the memory elements [Fig. 1A-1D]; an array configuration circuit for selectively placing the at least one array in one of two operating configurations [col. 2, ll 20-27]; a sub-array selector, responsive to a first memory address, for selecting one among the plurality of sub-arrays according to the first memory address, the sub-array selector enabling access to the selected sub-array [col. 2, ll 28-36]; and a memory element access circuit, responsive to a second memory address, for enabling access to a prescribed memory element in the selected sub-array after a prescribed number of shifts, depending on the second memory address, of the data content of the memory elements in the selected sub-array, the memory blocks of each sub-array being isolated from the memory blocks of the other sub-arrays [col. 22, lines 8-18, col. 33, lines 5-10, col. 33, lines 20-24], and a data content of any memory element of the sub-array being rotatable by shifts through the memory elements of the sub-array [col. 8, ll 36-50; col. 10, ll 29-42].

Iandaza does not specifically teach a first operating configuration, in which the memory elements of the at least one array are coupled one to another to form a monodimensional sequentially-accessible memory, and a second operating

configuration, in which the memory elements in each sub-array are coupled to one another so as to form an independent monodimensional sequentially-accessible memory block as required by the claim.

APA, however, discloses the two operating configurations including: a first operating configuration, in which the memory elements of the at least one array are coupled one to another to form a monodimensional sequentially-accessible memory, and a second operating configuration, in which the memory elements in each sub-array are coupled to one another so as to form an independent monodimensional sequentially-accessible memory block [pars. 6 and 7] to provide a memory that can be accessed sequentially in a first-in, first-out manner and a memory that can be accessed randomly (pars. 6-7).

Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Iadanza to include a first operating configuration, in which the memory elements of the at least one array are coupled one to another to form a monodimensional sequentially-accessible memory, and a second operating configuration, in which the memory elements in each sub-array are coupled to one another so as to form an independent monodimensional sequentially-accessible memory block since this would have provided a memory that can be accessed sequentially in a first-in, first-out manner and a memory that can be accessed randomly (pars. 6-7) as taught by APA.

Iadanza and APA do not explicitly disclose the first operating configuration is a data storage configuration, in which the memory is placed when data are to be stored

therein, and the second operating configuration is a data retrieval configuration, in which the memory is placed when data are to be retrieved therefrom.

Stone et al., however, discloses the first operating configuration is a data storage configuration, in which the memory is placed when data are to be stored therein [Fig. 10, *step 1010 read request?, yes/read, step 1026 random?, random: step 1034 read/retrieve data*; col. 9, lines 43-46, 58-64; Fig. 10, *step 1010 Read/Write Request?: if Yes/Read then step 1030: Retrieve Data Sequentially or step 1034: random retrieve data using address; or if Yes/write, then step 1018: random write data to address or step 1022: Write Data Sequentially*; col. 9, lines 36-64], and the second operating configuration is a data retrieval configuration, in which the memory is placed when data are to be retrieved therefrom [Fig. 10, *step 1010 write request, Yes/write, step 1022 write data sequentially*; col. 10, lines 8-12; Fig. 10, *step 1010 Read/Write Request?: if Yes/Read then step 1030: Retrieve Data Sequentially or step 1034: random retrieve data using address; or if Yes/write, then step 1018: random write data to address or step 1022: Write Data Sequentially*; col. 9, lines 36-64].

Thus, it would have been obvious to one of ordinary skill in the art, at the time of invention by applicant, to modify the system of Iadanza and APA, combined, to include the first operating configuration being a data storage configuration, in which the memory is placed when data are to be stored therein, and the second operating configuration being a data retrieval configuration, in which the memory is placed when data are to be retrieved therefrom because doing so would have enabled implementation of effective methods for optimizing and facilitating processor operations (col. 1, lines 60-61) as taught by Stone et al.

As per claim 2, Iadanza discloses said array configuration circuit includes, for each sub-array of memory elements, an input selector associated with a first memory element of the sub-array, for selectively feeding the first memory element with either an output of a last memory element in an adjacent previous sub-array, in the first operating configuration, or an output of a last memory element of the sub-array, in the second operating configuration [col. 2, ll 52-65; col. 5, ll 66 to col. 6, ll 12].

As per claim 4, Iadanza discloses in the second operating configuration each sub-array provides a respective output data, the sub-array selector selecting one sub-array output data out of the plurality of output data provided by the plurality of sub-arrays, according to the first address [col. 2, ll 28-36].

As per claim 5, Iadanza discloses said memory element access circuit enables a transfer of the output data of the selected sub-array to a memory output after a prescribed number of shifts of the data content of the memory elements in the selected sub-array [col. 8, ll 36-50; col. 10, ll 29-42].

As per claim 6, Iadanza discloses said memory element access circuit includes a counter for counting the number of data content shifts, and a coincidence detector detecting coincidence between a counter value and a value representative of the second address, the coincidence detector enabling the transfer of the output data of the

selected sub-array to the memory output when the counter value equals the value representative of the second address [col. 2, ll 36-44; col. 10, ll 10-28; col. 35, ll 34-51; col. 33, ll 25-34].

As per claim 7, Iadanza discloses each memory element includes at least one flip-flop [col. 28, ll 42-52].

17. Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomaiuolo (2002/0087817), Iadanza (6,091,645), and Stone et al. 6,578,109.

As per claim 12, Tomaiuolo discloses a memory, comprising: an array of memory locations [par. 005-006]; and a control circuit coupled to the array [page 6, left column, par. 8]; the memory locations comprise rings of serially coupled memory locations each having a respective contents with the contents of each ring being independent of the contents of the other rings [page 6, left column, par. 8].

Tomaiuolo does not explicitly teach during the first mode of operation, the control circuit is operable to control each of the rings to, receive a clock signal, shift the contents of each respective memory location in the ring to a respective next memory location in the ring once per cycle of the clock signal, and allow access to a predetermined one of the memory locations during a predetermined cycle of the clock signal.

Iadanza, however, discloses during the first mode of operation, the control circuit is operable to control each of the rings to, receive a clock signal, shift the contents of each respective memory location in the ring to a respective next memory location in the ring once per cycle of the clock signal, and allow access to a predetermined one of the memory locations during a predetermined cycle of the clock signal [col. 8, ll 36-50; col. 10, ll 29-42; col.11, ll 28-35; col. 35, ll 52-59] to provide serial scan shifting of data for driving each of the memory cells (col. 11, ll 30-35).

Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Tomaiuolo and APA to include shifting the contents of each respective memory location in the ring to a respective next memory location in the ring once per cycle of the clock signal since this would have provided serial scan shifting of data for driving each of the memory cells (col. 11, ll 30-35) as taught by Iadanza.

However, Tomaiuolo and Iadanza do not explicitly teach a control circuit operable to cause the array to operate as a random-access memory during all read operations and a first-in-first-out memory during all write operations.

Stone et al. discloses a control circuit operable to cause the array to operate as a random-access memory during all read operations [Fig. 10, *step 1010 read request?, yes/read, step 1026 random?, random: step 1034 read/retrieve data*; *if request is "Yes/Read" in step 1010 of Fig. 10, the controller 516 of Fig. 5 is operable to cause step 1026 to be "Random" for every read request to retrieve data*; col. 9, lines 43-46, 58-64; col. 9, lines 36-64] and a first-in-first-out memory during all write operations [Fig. 10, *step 1010 write request, Yes/write, step 1022 write*

data sequentially; col. 10, lines 8-12; Fig. 10, *step 1010 Read/Write Request?: if Yes/Read then step 1030: FIFO, Retrieve Data Sequentially or step 1034: if the Request is "Yes/Write" in step 1010 of Fig. 10, the controller 516 of Fig. 5 is operable to cause step 1014 to be "FIFO" for every write requests*; col. 9, lines 36-64].

Thus, it would have been obvious to one of ordinary skill in the art, at the time of invention by applicant, to modify the system of Tomaiuolo and Iadanza, combined, to include a control circuit operable to cause the array to operate as a random-access memory during all read operations and a first-in-first-out memory during all write operations because doing so would have enabled implementation of effective methods for optimizing and facilitating processor operations (col. 1, lines 60-61) as taught by Stone et al.

As per claim 13 Tomaiuolo discloses the memory locations comprise a ring of serially coupled memory locations each having a respective contents [page 6, left column, par. 8].

However, Tomaiuolo does not specifically teach during the first mode of operation, the control circuit is operable to, receive a clock signal, shifting the contents of each respective memory location in the ring to a respective next memory location in the ring once per cycle of the clock signal, and allow access to a predetermined one of the memory locations during a predetermined cycle of the clock signal.

Iadanza discloses during the read mode of operation, the control circuit is operable to, receive a clock signal, shifting the contents of each respective memory

location in the ring to a respective next memory location in the ring once per cycle of the clock signal, and allow access to a predetermined one of the memory locations during a predetermined cycle of the clock signal [col. 8, ll 36-50; col. 10, ll 29-42; col.11, ll 28-35; col. 35, ll 52-59] to provide serial scan shifting of data for driving each of the memory cells (col. 11, ll 30-35).

Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Tomaiuolo and Stone et al., combined, to include shifting the contents of each respective memory location in the ring to a respective next memory location in the ring once per cycle of the clock signal because doing so would have provided serial scan shifting of data for driving each of the memory cells (col. 11, ll 30-35) as taught by Iadanza.

Conclusion

18. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

19. When responding to the office action, Applicant is advised to clearly point out the patentable novelty that he or she thinks the claims present in view of the state of the art disclosed by references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111(c).

20. When responding to the Office action, Applicant is advised to clearly point out where support, with reference to page, line numbers, and figures, is found for any amendment made to the claims.

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MARDOCHEE CHERY whose telephone number is (571)272-4246. The examiner can normally be reached on 8:30A-5:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Mardochee Chery/
Examiner, Art Unit 2188

November 18, 2009